## REMARKS

This is in response to the Office Action dated December 14, 2004. New claim 42 has been added. Numerous non-elected claims have been canceled, without prejudice in view of the Restriction/Election Requirement. Thus, claims 9-15, 28, 35-37 and 42 are now pending.

Applicant notes with appreciation the Examiner's indication that claim 12 contains allowable subject matter. Allowable claim 12 has essentially been rewritten in independent form. Thus, given the Examiner's indication of allowable subject matter, claim 12 is now in condition for allowance.

*Claim 35 - Section 101 Double Patenting Rejection*

Claim 35 stands rejected under 35 U.S.C. Section 101 for alleged double patenting in view of 6,784,949. This Section 101 rejection is respectfully traversed for at least the following reasons. For example and without limitation, claim 10 of the '949 Patent requires that signal line, storage capacitor electrode and *common wire* are fabricated from a single electrode layer through patterning. Claim 35 of the instant application does not require this (there are other differences also). Thus, the inventions of instant claim 35 and '949 claim 10 are much different. The Section 101 double patenting rejection is incorrect and should be withdrawn.

*Claims 14-15*

Claims 14-15 stand rejected under 35 U.S.C. Section 103 as being allegedly unpatentable over Kakuda in view of Hibino. This Section 103 rejection is respectfully traversed for at least the following reasons. Hibino and the instant application are *commonly owned*, and were commonly owned at the time of the invention. This means that Hibino cannot be used in a 103

rejection. See 35 U.S.C. Section 103(c). The Section 103 rejection of claims 14-15 must be withdrawn. Thus, claims 14-15 are in condition for allowance.

*Claim 9 Defines Over Kakuda*

Claim 9 stands rejected under 35 U.S.C. Section 102(b) as being allegedly anticipated by Kakuda. This Section 102(b) rejection is respectfully traversed for at least the following reasons.

Claim 9 as amended requires "a storage capacitor common wire disposed parallel to the signal line so as to be electrically connected to the storage capacitor electrode, wherein storage capacitance is provided between the pixel electrode and the storage capacitor electrode, the scanning line and the storage capacitor electrode are fabricated from a same material in a single patterning; and wherein the storage capacitor electrode and the storage capacitor common wire are patterned in different steps so as to have an insulating film provided partially therebetween." For example and without limitation, see Figs. 18 and 24-25 of the instant application, which illustrate that the storage capacitor electrode 41 and the storage capacitor common wire 14 are patterned in different steps so as to have at least one insulating film 42 provided partially therebetween. In certain embodiments, the storage capacitor electrode 41 and the storage capacitor common wire 14 are electrically connected to each other via a contact hole 40 defined in the insulating film.

The cited art fails to disclose or suggest the aforesaid underlined aspect of claim 9. First, in direct contrast with claim 9, Kakuda teaches that the storage capacitor electrode 17 and the storage capacitor line 29 are formed at the *same time* in a *single patterning*. Kakuda in Fig. 8 show that the gate line 13 and the storage capacitance lines 29 are fabricated by patterning a single electrode (col. 10, lines 36-47). Thus, Kakuda fails to disclose or suggest that "the storage capacitor electrode and the storage capacitor common wire are patterned in different steps so as

to have an insulating film provided partially therebetween" as called for in claim 9. Second, in Kakuda the gate line 13 is thus parallel to the storage capacitance line 29, to prevent short-circuiting. In contrast with Kakuda, claim 9 requires that the storage capacitor common wire is disposed parallel to the signal line. For each of the aforesaid two reasons, Kakuda fails to disclose or suggest the invention of claim 9. Kakuda teaches the opposite of what amended claim 9 requires in each of these two respects.

*Claims 10 and 42*

Claim 10 stands rejected under Section 103(a) as being allegedly unpatentable over Kakuda in view of Shimada. This Section 103(a) rejection is respectfully traversed for at least the following reasons. Claim 10 (and new claim 42) requires that "the signal line and the pixel electrode are fabricated from a single conductive layer through patterning thereof."

The Office Action contends that the connecting electrode 7b in Figs. 2, 3 of Shimada correspond to the pixel electrode of claim 10. However, connecting electrode 7b in Figs. 2-3 of Shimada is not a pixel electrode, and the rejection of claim 10 is fundamentally flawed for at least this reason. For example, see Shimada at col. 5, lines 8-10 and col. 7, lines 59-61. Shimada is entirely unrelated to the invention of claim 10.

Thus, it is respectfully submitted that claims 10 and 42 defined over the cited art for at least these reasons.

*Conclusion*

For at least the foregoing reasons, the application is in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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